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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/207,745	12/08/98	SIMPKINS	D 32172-143271

WM02/0605

VENABLE
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WASHINGTON DC 20043-9998

EXAMINER	
TRAN, P	
ART UNIT	PAPER NUMBER
2664	8

DATE MAILED: 06/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/207,745	SIMPKINS ET AL.	
	Examiner	Art Unit	
	PHUC H TRAN	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 8 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 112

2. Claim 7 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Regarding to claim 7, "the said" in line 3 need to delete one of them.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, & 8-9 rejected under 35 U.S.C. 102(b) as being anticipated by Petersen (U.S. Patent No. 5430718, Jul. 4, 1995)

- With respect to claim 1, Petersen teaches a switch for switching time division multiplexed data and packet data from input ports to output ports (e.g. Fig. 2 shows the

time division switching with inputs and output), which comprises: a plurality of input ports receives data (e.g. block 10s in Fig. 2), wherein each data comprises either TDM data or packet data (e.g. packet data in time frame); a plurality of output ports transmits switched data (e.g. block 10m in Fig. 2); and a shared memory (e.g. block 4 in Fig. 2) couples the input ports to the output ports; the shared memory sequentially receives the data from the input ports; the shared memory switching sequentially receives data from a respective input port to a respective output port, wherein switching of packet data by the shared memory has no latency or jitter effect on switching of TDM data by the shared memory (e.g. data come from input and the switch memory sequentially receives data and sends to the output without delay).

- With respect to claim 2, Petersen also teaches each data is received by an input port as a time slot in a frame (col. 2, lines 65-66).

- With respect to claim 3, Petersen further teaches the shared memory, which comprises a TDM data memory portion and a packet data memory portion (e.g. the memory store packet data in time slot).

- With respect to claim 4, Petersen discloses the shared memory that treats the input ports as logical input ports (e.g. block 10s in Fig. 2).

- With respect to claim 5, Petersen teaches the shared memory places sequentially received packet data in a queue for a respective output port (e.g. data is received at the switch memory to transmit to the output).

- With respect to claim 6, Petersen also teaches the data are received by the input ports and transmitted by the output orts as data exchange units (e.g. the system of Petersen as exchange unit to transmit data from input to output port).

- With respect to claim 8, Petersen teaches the switching of a data from a respective input port to a respective output port is controlled by a stored switch configuration (it is inherently to know the control unit 20 in Fig. 2 for control the switching of data from input to output).

- With respect to claim 9, Petersen also teaches an input data router sequentially routing data from the input ports to the shared memory; and an output data router sequentially routing data from the shared memory to the output (e.g. Fig. 2 shows the input and output connect to the memory).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen (U.S. Patent No. 5430718, Jul. 4, 1995) in view of Ferenc et al. (U.S. Patent No. 4731785, Mar. 15, 1988).

- With respect to claim 7, Petersen teaches a time division switch and fails to teach a time slot interchange controller couples to the shared memory selecting

addresses in the shard memory to store TDM data, the time slot interchange controller selecting an address of the shared memory for a TDM data based on a time slot of a frame in which the switch received the TDM data; and a packet switch controller couples to the shared memory selecting addresses in the shard memory to store packet data, the packet switch controller selecting an address of shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data. Ferenc discloses the controller (block 104 in Fig. 1), which operates on a time slot by time slot basis and the packet controller (block 305 in Fig. 3), which control the packet to the memory and to the output. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use the controller and the packet controller of Ferenc into Petersen's invention to control the time frame and packet data from input port to send to output port.

7. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen (U.S. Patent No. 5430718, Jul. 4, 1995) in view of Hayano (U.S. Patent No. 4941141, Jul. 10, 1990).

- With respect to claims 10 & 13, Petersen teaches switching time division multiplexed data and packet data from input ports to output ports (e.g. Fig. 2 shows the time division switching with inputs and output), which comprises the steps of: switching a TDM data from an input port to an output port that comprises the steps of: receiving a TDM data at the input port (e.g. block 10s in Fig. 2); determining the output port to route the TDM data (e.g. the data is routing and determining the output port at the control);

storing the TDM data in a shared memory (e.g. block 4 in Fig. 2); reading the TDM data from the shared memory (e.g. the control memory reads out data from the memory); transmitting the TDM data from the output port (e.g. block 10m in Fig. 2); and switching a packet data from an input port to an output port, which comprises the steps of: receiving a packet data at the input port (e.g. block 10s in Fig. 2); determining the output port to route the packet data; storing the packet data in the shared memory (e.g. block 4 in Fig. 2); reading the packet data from the shared memory (e.g. the control memory reads out data from the memory); and transmitting the packet data from the output port (e.g. block 10m in Fig. 2); wherein switching packet data has no latency or jitter effect on switching TDM data (e.g. data come from input and the switch memory sequentially receives data and sends to the output without delay). Petersen fails to teach the preselected area of memory for storing and reading data. Hayano discloses the preselected area of memory (blocks 104, 105 in Fig. 3) to store data information in different area for easy to access and control the data in the memory. Therefore, it would have obvious to a person of ordinary skill in the art at the time of the invention was made to use the memory with preselected area for control and access the data information in the switching system.

- With respect to claim 11, Petersen fails to teach the preselected area of memory for storing the TDM data is based on a time slot in a frame. Hayano discloses the preselected area of memory (blocks 104, 105 in Fig. 3) to store data information, which bases on the time slot in a frame (col. 4, lines 20-37), in different area for easy to access and control the data in the memory. Therefore, it would have obvious to a

person of ordinary skill in the art at the time of the invention was made to use the memory with preselected area for control and access the data information in the switching system.

- With respect to claim 12, Petersen also teaches the output port to which the TDM data is routed is determined based on a time slot in a frame in which the TDM data was received by the input port, and wherein the output port to which the packet data is routed is determined based on routing data embedded in the packet data and based on the input port which received the packet data (e.g. the data from input ports is determined to send to the output ports base on the times and the destination information).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Endo et al. (U.S Patent No. 4964119) discloses method and system form packet exchange.
- Chao et al. (U.S Patent No. 4893306) discloses method and apparatus for multiplexing circuit and packet traffic.
- Sakurai et al. (U.S Patent No. 6215788 B1) discloses ATM cell switching system.
- Kosuge et al. (U.S Patent No. 4575844) discloses digital switching system.
- Shively (U.S Patent No. 5978370) discloses circuit-switched switching system.
- Closs et al. (U.S Patent No. 3796835) discloses switching system for TDM data which induces an asynchronous submultiplex channel.
- Sakurai et al. (U.S Patent No. 5995510) discloses distributed type switching system.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUC H TRAN whose telephone number is (703) 308-7471. The examiner can normally be reached on M-F (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WELLINGTON CHIN can be reached on (703) 305-4366. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 872-9314.

Phuc Tran
Assistant Examiner
Art Unit 2664

P.t
May 29, 2001

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